What is claimed is:

1. A semiconductor device, comprising:

a semiconductor substrate of a first conductivity; and

a semiconductor layer provided on the semiconductor substrate and having a super junction structure including drift layers of the first conductivity and RESURF layers of a second conductivity different from the first conductivity, the drift layers and the RESURF layers being laterally arranged in alternate relation in a direction parallel to the semiconductor substrate, wherein

the RESURF layers are each provided alongside an interior side wall of a trench penetrating through the semiconductor layer, and

the drift layers each have an isolation region present between the RESURF layer and the semiconductor substrate to prevent the RESURF layer from contacting the semiconductor substrate.

2. A semiconductor device as set forth in claim 1, wherein

the RESURF layers are each provided alongside one of widthwise opposite interior side walls of the trench,

the drift layers are each provided alongside the other of the widthwise opposite interior side walls of the trench, and

a width of a portion of the drift layer between the trench and the RESURF layer as measured laterally is nearly equal to a width of the isolation region as measured vertically depthwise of the trench.

3. A semiconductor device as set forth in claim 1, wherein

the RESURF layers are provided alongside widthwise opposite interior side walls of the trenches, and

a width of a portion of the drift layer between two adjacent RESURF layers as measured laterally is generally double a width of the isolation region as measured vertically depthwise of the trench.

4. A semiconductor device as set forth in any of claims 1 to 3, further comprising:

base regions of the second conductivity each provided in contact with the drift layer and the RESURF layer;

source regions of the first conductivity each provided in contact with the base region and isolated from the drift layer and the RESURF layer by the base region; and

gate electrodes each provided in opposed relation to a portion of the base region between the source region and the drift layer with the intervention of a gate insulation film.

5. A production method for a semiconductor device which includes a semiconductor layer provided on a semiconductor substrate of a first conductivity and having a super junction structure including drift layers of the first conductivity and RESURF layers of a second conductivity different from the first conductivity, the drift layers and the RESURF layers being laterally arranged in alternate relation in a direction parallel to the semiconductor substrate, the production method comprising the steps of:

forming a semiconductor layer of the first conductivity on a semiconductor substrate of the first conductivity;

performing a first trench formation process to form a trench in the semiconductor layer, the trench having a depth such as to reach a middle of the semiconductor layer;

after the first trench formation step, performing an in-trench impurity introduction process to introduce an impurity of the second conductivity into a portion of the semiconductor layer exposed to an interior side wall of the trench for forming a RESURF layer of the second conductivity alongside the interior side wall of the trench; and

after the in-trench impurity introduction step, performing a second trench formation process to deepen

the trench to a depth such as to penetrate through the semiconductor layer to reach the semiconductor substrate.

6. A production method for a semiconductor device which includes a semiconductor layer provided on a semiconductor substrate of a first conductivity and having a super junction structure including drift layers of the first conductivity and RESURF layers of a second conductivity different from the first conductivity, the drift layers and the RESURF layers being laterally arranged in alternate relation in a direction parallel to the semiconductor substrate, the production method comprising the steps of:

forming a semiconductor layer of the first conductivity on a semiconductor substrate of the first conductivity;

forming a trench in the semiconductor layer, the trench penetrating through the semiconductor layer to reach the semiconductor substrate; and

performing an in-trench impurity introduction process to implant an impurity of the second conductivity at an inclination angle into a portion of the semiconductor layer exposed to an interior side wall of the trench for forming a RESURF layer of the second conductivity in the portion of the semiconductor layer alongside the interior side wall of the trench, the inclination angle being such that the impurity reaches a limited depthwise range of

the interior side wall of the trench shallower than the semiconductor substrate.

7. A semiconductor device production method as set forth in claim 5 or 6, wherein

the in-trench impurity introduction step includes the step of performing an implantation process to implant the impurity of the second conductivity into a surface portion of the semiconductor layer exposed to the interior side wall of the trench,

the production method further comprising the step of performing a thermal diffusion process to heat the resulting semiconductor substrate after the implantation step for diffusing the implanted impurity into the semiconductor layer for the formation of the RESURF layer.

8. A semiconductor device production method as set forth in any of claims 5 to 7, further comprising the steps of:

introducing an impurity of the second conductivity into a surface portion of the semiconductor layer to form a base region of the second conductivity in contact with the RESURF layer;

introducing an impurity of the first conductivity into a portion of the base region to form a source region of the first conductivity which is isolated from the drift layer and the RESURF layer by a remaining portion of the

base region;

forming a gate insulation film opposed to the portion of the base region between the source region and the drift layer; and

forming a gate electrode opposed to the portion of the base region between the source region and the drift layer with the intervention of the gate insulation film.